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1. **VERILAT: verification using logic augmentation and transformations**
   Paul, D.; Chatterjee, M.; Pradhan, D.K.;
   Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions
   Volume 19, Issue 9, Sept. 2000 Page(s):1041 - 1051
   Digital Object Identifier 10.1109/43.863644
   AbstractPlus | References | Full Text: PDF(300 KB) IEEE JNL
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2. **PECS: a peak current and power simulator for CMOS combinational circuit**
   Lam, K.N.; Devadas, S.;
   Circuits and Systems, 1996. ISCAS '96., 'Connecting the World', 1996 IEEE Inte
   Symposium on
   Volume 4, 12-15 May 1996 Page(s):488 - 491 vol.4
   Digital Object Identifier 10.1109/ISCAS.1996.542007
   AbstractPlus | Full Text: PDF(316 KB) IEEE CNF
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3. **An efficient perfect algorithm for memory repair problems**
   Hung-Yau Lin; Fu-Min Yeh; Ing-Yi Chen; Sy-Yen Kuo;
   Defect and Fault Tolerance in VLSI Systems, 2004. DFT 2004. Proceedings. 19t
   International Symposium on
   10-13 Oct. 2004 Page(s):306 - 313
   Digital Object Identifier 10.1109/DFTVS.2004.1347853
   AbstractPlus | Full Text: PDF(705 KB) IEEE CNF
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4. **A Boolean algebra method for computing the terminal reliability in a comm network**
   Fratta, L.; Montanari, U.;
   Circuits and Systems, IEEE Transactions on [legacy, pre - 1988]
   Volume 20, Issue 3, May 1973 Page(s):203 - 211
   AbstractPlus | Full Text: PDF(896 KB) IEEE JNL
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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	5120	(duplicat$4 or replicat$4) with (flip-flop or (flip adj flop) or register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:06
L2	10722	statis$6 same circuit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:06
L3	468	(statis$6 same circuit) same transform$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:06
L4	35	(duplicat$4 or replicat$4) with (flip-flop or (flip adj flop) or register) and rtl and test	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:06
L5	3	(duplicat$4 or replicat$4) with (flip-flop or (flip adj flop) or register) and (statist$5 near4 circuit)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:06
L6	49	(duplicat$4 or replicat$4) with (flip-flop or (flip adj flop) or register) and transform$4 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:06
L7	37	(duplicat$4 or replicat$4) with (flip-flop or (flip adj flop) or register) and rtl and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:06
L8	18	(duplicat$4 or replicat$4) with (flip-flop or (flip adj flop) or register) and rtl and node and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:06

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L9	32	(duplicat$4 or replicat$4) with (flip-flop or (flip adj flop) or register) and rtl and port$3 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:06
L10	49	(duplicat$4 or replicat$4) with (flip-flop or (flip adj flop) or register) and rtl and port$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:06
L11	64	(duplicat$4 or replicat$4) with (flip-flop or (flip adj flop) or register) and rtl	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:06
L12	34	((statis$6 same circuit) same transform$5) and node and portion	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:08
L13	23	(((statis$6 same circuit) same transform$5)) and ("716"/$.ccls. or "710"/$.ccls. or "712"/$.ccls.) and statis$6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:06
L14	23	(((statis$6 same circuit) same transform$5)) and ("716"/$.ccls. or "710"/$.ccls. or "712"/$.ccls.) and statis$6 and transform$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:06
L15	121	(duplicat$4 or replicat$4) with (flip-flop or (flip adj flop) or register) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:06
L16	406	(duplicat$4 or replicat$4) with (flip-flop or (flip adj flop) or register) and transform$4 and node	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:06

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L17	2	((statis$6 same circuit) same transform$5) and node and portion and (rtl or register adj transfer adj level)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:06
L18	2	((statis$6 same circuit) same transform$5) and node and (rtl or register adj transfer adj level)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:06
L19	2	((statis$6 same circuit) same transform$5) and node and (rtl or (register adj transfer adj level))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:06
L20	9	((statis$6 same circuit) same transform$5) and node and boolean	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:07
L21	15	((statis$6 same circuit) same transform$5) and boolean	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:07
L22	14	((statis$6 same circuit) same transform$5) and node and portion and circuit and data and gate	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:10
L23	0	(((statis$6 same circuit) same transform$5) and node and portion and circuit and data and gate).CLM.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:10

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L23	0	(((statis$6 same circuit) same transform$5) and node and portion and circuit and data and gate).CLM.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/10 13:10